

ABSTRACT OF THE DISCLOSURE

A method of identifying line width errors in an integrated circuit design includes adding a line width marker for each of a plurality of lines on a schematic, each line having a schematic line width, creating a layout from the schematic, the layout containing the line width markers and a plurality of layout widths, checking the layout line widths versus the schematic line widths for the plurality of line width marked lines, creating a design representing the layout, the design having a plurality of design line widths, and checking the design line widths versus the layout line widths for the plurality of line width marked lines.